
IN THE CLAIMS

1. (Original) An integrated circuit comprising:
control circuitry to place the integrated circuit in a test mode;
a reset connection to receive an externally provided active low reset signal to reset the integrated circuit, the reset connection can receive an elevated voltage during the test mode; and
an input buffer circuit coupled to the reset connection.
2. (Original) The integrated circuit of claim 1 wherein the integrated circuit further comprises a pull-up bias circuit coupled to the reset connection, wherein the pull-up bias circuit is active only during the test mode.
3. (Original) The integrated circuit of claim 2 wherein the pull-up bias circuit comprises an n-channel transistor coupled between the reset connection and a voltage supply, Vcc, a gate of the transistor is selectively coupled to Vcc during the test mode.
4. (Original) A synchronous non-volatile memory device comprising:
an array of non-volatile memory cells;
control circuitry to place the memory device in a test mode in response to an external test command;
a supply connection to receive a voltage supply, Vcc;
a reset connection to receive an externally provided active low reset signal to reset the memory device, the reset connection can receive an elevated voltage during the test mode, where the elevated voltage is greater than Vcc; and
an input buffer circuit coupled to the reset connection.
5. (Original) The synchronous non-volatile memory device of claim 4 wherein the synchronous non-volatile memory device further comprises a pull-up bias circuit coupled to the reset connection, wherein the pull-up bias circuit is active only during the test mode.

6. (Original) The synchronous non-volatile memory device of claim 5 wherein the pull-up bias circuit comprises an n-channel transistor coupled between the reset connection and Vcc, a gate of the transistor is selectively coupled to Vcc during the test mode.
7. (Currently Amended) A method of operating an integrated circuit comprising:
initiating a test operation of the integrated circuit; and
activating a bias circuit coupled to a reset connection of the integrated circuit during the test operation to bias the reset connection, wherein the reset connection can receive an elevated voltage during the test operation, where the elevated voltage is greater than Vcc.
8. (Original) The method of claim 7 wherein the reset connection is coupled to receive an active low reset signal during normal operation.
9. (Currently Amended) ~~The method of claim 8~~ A method of operating an integrated circuit comprising:
initiating a test operation of the integrated circuit; and
activating a bias circuit coupled to a reset connection of the integrated circuit during the test operation;
wherein the reset connection is coupled to receive an active low reset signal during normal operation;
wherein the bias circuit is a pull-up circuit coupled to prevent the reset connection from floating during the test operation.
10. (Currently Amended) ~~The method of claim 7~~ A method of operating an integrated circuit comprising:
initiating a test operation of the integrated circuit; and
activating a bias circuit coupled to a reset connection of the integrated circuit during the test operation;
wherein activating the bias circuit comprises coupling a supply voltage, Vcc, to a gate of a pull-up transistor coupled between the reset connection and Vcc.

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11. (Currently Amended) ~~The method of claim 7~~ A method of operating an integrated circuit comprising:
initiating a test operation of the integrated circuit;
activating a bias circuit coupled to a reset connection of the integrated circuit during the
test operation; and
coupling an elevated voltage supply to the reset connection, wherein the elevated voltage supply is greater than a voltage supply, Vcc.
12. (Original) A method of operating an integrated circuit device comprising:
activating a pull-up bias circuit coupled to a reset connection of the integrated circuit device;
coupling active low reset signals to the reset connection during a test operation using a first tester;
disconnecting the first tester from the reset connection; and
coupling an elevated supply voltage to the reset connection.
13. (Original) The method of claim 12 wherein the pull-up bias circuit is internal to the integrated circuit device.
14. (Original) The method of claim 12 wherein the pull-up bias circuit is activated during the test operation and deactivated in non-test operations.
15. (Original) The method of claim 12 further comprises initiating a test operation of the memory device via external commands.
16. (Original) A method of operating an integrated circuit comprising:
initiating a test operation of the integrated circuit via externally provided commands;
activating an internal pull-up bias circuit coupled to a reset connection of the integrated circuit;
coupling active low reset signals to the reset connection during a test operation using a first tester;

disconnecting the first tester from the reset connection such that the reset connection is not actively driven from an outside source, wherein the activated pull-up bias circuit prohibits a voltage on the reset connection from transitioning to a low state; and coupling an elevated supply voltage to the reset connection during the test operation, wherein the elevated voltage supply is greater than an operating voltage supply, V_{cc} .

17. (Original) An integrated circuit comprising:
 - control circuitry to place the integrated circuit in a test mode in response to an external test command;
 - a supply connection to receive a voltage supply, V_{cc} ;
 - a reset connection to receive an externally provided active low reset signal to reset the integrated circuit;
 - an input buffer circuit coupled to the reset connection; and
 - a pull-up circuit coupled to the reset connection, wherein the pull-up circuit is active only during the test mode, the pull-up circuit comprises,
 - a current limiting resistor coupled to the reset connection, and
 - a transistor coupled between the resistor and V_{cc} .
18. (Original) A system comprising:
 - a processor; and
 - a memory device coupled to the processor, the memory device comprising:
 - control circuitry to place the memory device in a test mode in response to an external test command,
 - a supply connection to receive a voltage supply, V_{cc} ,
 - a reset connection to receive an externally provided active low reset signal to reset the memory device,
 - an input buffer circuit coupled to the reset connection, and
 - a pull-up circuit coupled to the reset connection, wherein the pull-up circuit is active only during the test mode, the pull-up circuit comprises,
 - a current limiting resistor coupled to the reset connection, and
 - a transistor coupled between the resistor and V_{cc} .

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19. (Original) A test system comprising:
- a first and second test devices; and
 - a memory device selectively coupled to either the first or second test devices, the memory device comprising:
 - control circuitry to place the memory device in a test mode in response to an external test command,
 - a supply connection to receive a voltage supply, V_{cc} ,
 - a reset connection to receive an externally provided active low reset signal to reset the memory device,
 - an input buffer circuit coupled to the reset connection, and
 - a pull-up circuit coupled to the reset connection, wherein the pull-up circuit is active only during the test mode, the pull-up circuit comprises,
 - a current limiting resistor coupled to the reset connection, and
 - a transistor coupled between the resistor and V_{cc} .